IN THE CLAIMS:

Claim 1. (Original) A method for the production of a semiconductor component provided with a first vertical power component (5,9) and at least one lateral, active component (6) and/or at least one second vertical power component (10) having the steps:

- provision of a silicon substrate (1) having a front side and a back side,

etching into said silicon substrate (1) at least one
trench (2), which completely encompasses at least a part of said front side,

- filling said at least one trench (2) with an insulation (4), which contains at least one dielectric or is a dielectric,

- conducting process steps on said front side of said silicon substrate (1) to produce a first vertical power component (5,9) and at least one lateral, active component (6) and/or at least one second vertical power component (10) in such a manner that on said substrate (1) said first power component (5,9) and said at least one lateral, active component (6) and/or said at least one second vertical power component (10) are arranged concentrically or eccentrically around a common point of reference and are separated from each other by at least one said trench (2),

- thinning the entire surface of said silicon substrate (1) from said back side to said insulation (4),

- contacting said power components (5,9,10) from said back side.

Claim 2. (Original) A method according to claim 1,
wherein

said first power component (5,9), said at least one lateral, active component (6) and/or said at least one second vertical power component (10) are designed approximately ring-shaped and/or disk-shaped.

Claim 3. (Currently Amended) A method according to claim 1 ~~or 2~~,
wherein

said lateral, active component (6) is designed disk-shaped and is placed on said front side in such a manner that it is completely encompassed by said trench (2) and said first vertical power component (5,9).

Claim 4. (Currently Amended) A method according to ~~one of the claims 1 to 3~~ claim 1,

wherein
after said thinning and before said contacting of said at least one power component (5,9) a dielectric is deposited on said back side of said substrate (1).

Claim 5. (Original) A method according to claim 4,
wherein said contacting of said power component (5,9)
comprising the steps:
- production of openings in said dielectric for contacting said at least one power component (5,9) from said back side

and

- application of a metalization (8) on said back side.

Claim 6. (Original) A method according to claim 5,
wherein said metallization (8) is structured.

Claim 7. (Currently Amended) A method according to ~~one of the claims 1 to 6,~~ claim 1
wherein said at least one lateral, active component (6) is placed in a doped trough.

Claim 8. (Original) A method according to claim 7,
wherein said at least one lateral, active component (6) is placed in a p-doped trough.

Claim 9. (Currently Amended) A method according to ~~one of the claims 1 to 8~~ claim 1,
wherein said at least one lateral, active component (6) is integrated in said semiconductor component by means of Bipolar, CMOS, NMOS and/or PMOS technology.

Claim 10. (Original) A semiconductor component comprising at least one first vertical power component (5,6) and at least one lateral, active component (6) and/or at least one second vertical power component (10), between which at least one trench (2) filled with an insulation (4) is placed,
wherein
said insulation (4) comprises at least partly one dielectric and said at least one vertical power component (5,9) and said at least one lateral, active component (6) are designed approximately ring-shaped and/or disk-shaped and are arranged eccentrically or concentrically around a common point of reference on a silicon substrate (1).

Claim 11. (Original) A semiconductor component according to claim 10,
wherein said at least one power component (5,9) is an IGBT, a PMOS and/or a diode.

Claim 12. (Currently Amended) A semiconductor component according to claim 10 ~~or 11~~, wherein said at least one power component (5,9) is suited for voltages of up to 1700 V.

Claim 13. (Currently Amended) A semiconductor component according to ~~one of the claims 10 to 12~~ claim 10, wherein said insulation (4) is composed of a combination of insulating, semiconducting and/or conducting materials.

Claim 14. (Currently Amended) A semiconductor component according to ~~one of the claims 10 to 13~~ claim 10,
wherein said insulation (4) is composed of a combination of a dielectric and polysilicon.

Claim 15. (Currently Amended) A semiconductor component according to ~~one of the claims 10 to 14~~ claim 10,
wherein said first vertical power component (5,9) and/or said at least one lateral, active component (6) is completely encompassed by at least one filled trench (2) and/or said at least one second vertical power component (10).

Claim 16. (Currently Amended) A semiconductor component according to ~~one of the claims 10 to 15~~ claim 10,
wherein said at least one lateral, active component (6) is placed in a doped trough.

Claim 17. (Currently Amended) A semiconductor component according to ~~one of the claims 10 to 16~~ claim 10,
wherein a dielectric is applied on the back side of said semiconductor component.

Claim 18. (Original) A semiconductor component according to claim 17,
wherein
said dielectric is provided with openings through which said power components (5,9,10) are contactable.